CLAIMS

What is claimed is:

1. A microelectronic substrate, comprising:

a first microelectronic substrate core having a first surface and an opposing second surface, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface;

at least one first microelectronic device disposed within said at least one opening, said at least one first microelectronic device having an active surface and a back surface, wherein said first microelectronic device active surface is adjacent said first microelectronic substrate core first surface;

an encapsulation material adhering said first microelectronic substrate core to said at least one first microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface and a second surface adjacent said microelectronic die back surface and said core second surface; and

at least one conductive via extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface.

2. The microelectronic substrate of claim 1, further including a first interconnection layer disposed proximate said first microelectronic substrate core first surface and said first microelectronic device active surface and further including a second interconnection layer disposed proximate said first microelectronic substrate core second

surface and said first microelectronic device back surface, wherein said at least one conductive via electrically connects said first interconnection layer and said second interconnection layer.

3. The microelectronic substrate of claim 2, further including at least one microelectronic device attached to at least one of said first interconnection layer and said second interconnection layers.

4. The microelectronic substrate of claim 2, further including at least one heat dissipation device thermally attached to said at least one microelectronic device back surface.

5. The microelectronic substrate of claim 2, wherein said first interconnection layer comprises at least one dielectric layer abutting at least one of said first microelectronic device active surface, said first microelectronic substrate core first surface, and said encapsulation material first surface, and at least one conductive trace disposed on said at least one dielectric layer.

6. The microelectronic substrate of claim 5, wherein said at least one conductive trace extends through said at least one dielectric layer to contact at least one electrical contact on said first microelectronic device active surface.

7. The microelectronic substrate of claim 5, wherein said at least one conductive trace extends through said at least one dielectric layer to contact said at least one conductive via.

8. The microelectronic substrate of claim 2, wherein said second interconnection layer comprises at least one dielectric layer abutting at least one of said microelectronic device back surface, said microelectronic substrate core second surface, and said encapsulant material second surface, and at least one conductive trace disposed on said at least one dielectric layer.

9. The microelectronic substrate of claim 8, wherein said at least one conductive trace extends through said at least one dielectric layer to contact said at least one conductive via.

10. The microelectronic substrate of claim 1, further including:

a second microelectronic substrate core having a first surface and an opposing second surface, said second microelectronic substrate core having at least one opening defined therein extending from said second microelectronic substrate core first surface to said second microelectronic substrate core second surface;

at least one second microelectronic device disposed within said at least one opening, said at least one second microelectronic device having an active surface

adjacent said second microelectronic substrate core first surface and a back surface adjacent said second microelectronic substrate core second surface;

an encapsulation material adhering said second microelectronic substrate core to said at least one second microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface and a second surface adjacent said microelectronic die back surface and said core second surface;

said first microelectronic substrate core second surface attached to said second microelectronic substrate core second surface; and

said at least one conductive via extends from said first microelectronic substrate core first surface to said second microelectronic substrate core first surface.

11. The microelectronic substrate of claim 10, further including a heat dissipation device disposed between said first microelectronic substrate core second surface and said second microelectronic substrate core second surface.

12. The microelectronic substrate of claim 11, further including a dielectric material disposed between said conductive via and said heat dissipation device.

13. A microelectronic substrate, comprising:

at least one first microelectronic device having an active surface and a back surface;

an encapsulation material forming a first surface adjacent said microelectronic die active surface and a second surface adjacent said microelectronic die back surface; and

at least one conductive via extending from said encapsulation material first surface to said encapsulation material second surface.

14. The microelectronic substrate of claim 13, further including a first interconnection layer disposed proximate said encapsulation material first surface and said first microelectronic device active surface and further including a second interconnection layer disposed proximate said encapsulation material second surface and said first microelectronic device back surface, wherein said at least one conductive via electrically connects said first interconnection layer and said second interconnection layer.

15. A microelectronic substrate, comprising:

a first microelectronic substrate core having a first surface and an opposing second surface, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface;

at least one first microelectronic device disposed within said at least one opening, said at least one first microelectronic device having an active surface and a back surface, wherein said first microelectronic device active surface is adjacent said first microelectronic substrate core first surface;

a first encapsulation material adhering said first microelectronic substrate core to said at least one first microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface and a second surface adjacent said microelectronic die back surface and said core second surface;

a second microelectronic substrate core having a first surface and an opposing second surface, said second microelectronic substrate core having at least one opening defined therein extending from said second microelectronic substrate core first surface to said second microelectronic substrate core second surface;

at least one second microelectronic device disposed within said at least one opening, said at least one second microelectronic device having an active surface and a back surface, wherein said second microelectronic device active surface is adjacent said second microelectronic substrate core first surface;

a second encapsulation material adhering said second microelectronic substrate core to said at least one second microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface and a second surface adjacent said microelectronic die back surface and said core second surface; and

said first microelectronic device active surface oriented to face said second microelectronic device active surface.

16. The microelectronic substrate of claim 15, further including a first interconnection layer disposed proximate said first microelectronic substrate core first surface, said first encapsulation first surface, and said first microelectronic device active

surface and further including a second interconnection layer disposed proximate said second microelectronic substrate core first surface, said second encapsulation material first surface, and said first microelectronic device active surface, wherein said first and second interconnection layers are electrically connected.

17. The microelectronic substrate of claim 15, further including an interconnection layer disposed proximate at least one of said first microelectronic substrate core second surface, said first encapsulation material second surface, and said first microelectronic device back surface, and said second microelectronic substrate core second surface, said second encapsulation material second surface, and said second microelectronic device back surface.

18. The microelectronic substrate of claim 15, further including at least one conductive via extending from said first microelectronic substrate core first surface and said first microelectronic substrate core second surface.

19. The microelectronic substrate of claim 15, further including at least one conductive via extending between said second microelectronic substrate core first surface and said second microelectronic substrate core second surface.

20. The microelectronic substrate of claim 15, further including at least one conductive via extending from said first microelectronic substrate core second surface and said second microelectronic substrate core second surface.

21. The microelectronic substrate of claim 15, further including at least one heat dissipation device thermally attached to at least one of said at least one first microelectronic device back surface and said at least one second microelectronic device back surface.

22. A microelectronic substrate, comprising:

a first microelectronic substrate core having a first surface and an opposing second surface, said first microelectronic substrate core having at least one cavity defined therein;

at least one first microelectronic device disposed within said at least one cavity, said at least one first microelectronic device having an active surface and a back surface, wherein said first microelectronic device active surface is adjacent said first microelectronic substrate core first surface;

a first encapsulation material adhering said first microelectronic substrate core to said at least one first microelectronic device forming a first surface adjacent said microelectronic die active surface;

a second microelectronic substrate core having a first surface and an opposing second surface, said second microelectronic substrate core having at least one cavity defined therein;

at least one second microelectronic device disposed within said at least one cavity, said at least one second microelectronic device having an active surface and a back surface, wherein said second microelectronic device active surface is adjacent said second microelectronic substrate core first surface;

a second encapsulation material adhering said second microelectronic substrate core to said at least one second microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface; and

said first microelectronic device active surface oriented to face said second microelectronic device active surface.

23. The microelectronic substrate of claim 22, further including a first interconnection layer disposed proximate said first microelectronic substrate core first surface, said first encapsulation first surface, and said first microelectronic device active surface and further including a second interconnection layer disposed proximate said second microelectronic substrate core first surface, said second encapsulation material first surface, and said first microelectronic device active surface, wherein said first and second interconnection layers are electrically connected.

24. A method of fabricating a microelectronic substrate, comprising:

providing a first microelectronic substrate core having a first surface and an opposing second surface, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface;

disposing at least one first microelectronic device having an active surface and a back surface within said at least one opening such that said first microelectronic device active surface resides adjacent said first microelectronic substrate core first surface;

disposing an encapsulation material in said at least one opening to adhere said first microelectronic substrate core to said at least one first microelectronic device and forming a first surface adjacent said microelectronic die active surface and a second surface adjacent said microelectronic die back surface; and

forming at least one conductive via to extend from said first microelectronic substrate core first to said first microelectronic substrate core second surface.

25. The method of claim 24, further including thermally attaching at least one heat dissipation device to at least one microelectronic device back surface.

26. The method of claim 24, further including:

forming a first interconnection layer disposed proximate said first microelectronic substrate core first surface, said encapsulation material first surface, and said first microelectronic device active surface;

forming a second interconnection layer disposed proximate said first microelectronic substrate core second surface, said encapsulation material second surface, and said first microelectronic device back surface.

27. The method of claim 26, wherein forming said first interconnection layer comprises:

forming at least one dielectric material layer on at least a portion of said first microelectronic device active surface, said encapsulation material first surface, and said microelectronic substrate core first surface;

forming at least one via through said at least one dielectric material layer to expose a portion of said microelectronic device active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said at least one via to electrically contact said first microelectronic device active surface.

28. The method of claim 27, wherein forming at least one conductive trace comprises forming said at least one conductive trace to extend through said at least one dielectric layer to contact said at least one conductive via.

29. The method of claim 26, wherein forming said second interconnection layer comprises:

forming at least one dielectric material layer on at least a portion of said first microelectronic device back surface, said encapsulation material second surface, and said microelectronic substrate core second surface;

forming at least one via through said at least one dielectric material layer; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said at least one via to electrically contact said conductive via.

30. The method of claim 24, further including:

providing a second microelectronic substrate core having a first surface and an opposing second surface, said second microelectronic substrate core having at least one opening defined therein extending from said second microelectronic substrate core first surface to said second microelectronic substrate core second surface;

disposing at least one second microelectronic device within said at least one opening, such that an active surface of said at least one second microelectronic device resides adjacent said second microelectronic substrate core first surface and such that a back surface of said at least one second microelectronic device resides adjacent said second microelectronic substrate core second surface;

disposing an encapsulation material in said opening to adhere said second microelectronic substrate core to said at least one second microelectronic device;

attaching said first microelectronic substrate core second surface to said second microelectronic substrate core second surface; and

forming said at least one conductive via to extend from said first microelectronic substrate core first surface to said second microelectronic substrate core first surface.

31. The method of claim 30, further including disposing a heat dissipation device between said first microelectronic substrate core second surface and said second microelectronic substrate core second surface.

32. The method of claim 30, further including forming at least one conductive via interconnecting said first microelectronic substrate core first surface and said second microelectronic substrate core first surface.

33. The method of claim 32, further including disposing a dielectric material between said at least one conductive via and said heat dissipation device.

34. The method of claim 24, further including abutting said first microelectronic substrate core first surface and said first microelectronic device active surface against a protective film prior to disposing said encapsulation material in said at least one opening.

35. The method of claim 34, wherein abutting said microelectronic substrate core first surface and said at least one microelectronic device active surface against a protective film comprises abutting said first microelectronic substrate core first surface

and said first microelectronic device active surface against an adhesive layer on said protective film prior to disposing said encapsulation material in said at least one opening.

36. A method of fabricating a microelectronic substrate, comprising:

providing a first microelectronic substrate core having a first surface and an opposing second surface, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface;

disposing at least one first microelectronic device having an active surface and a back surface within said at least one opening such that said first microelectronic device active surface resides adjacent said first microelectronic substrate core first surface;

disposing a first encapsulation material in said microelectronic substrate core opening adhering said first microelectronic substrate core to said at least one first microelectronic device, forming a first surface adjacent said first microelectronic die active surface and a second surface adjacent said first microelectronic die back surface;

providing a second microelectronic substrate core having a first surface and an opposing second surface, said second microelectronic substrate core having at least one opening defined therein extending from said second microelectronic substrate core first surface to said second microelectronic substrate core second surface;

disposing at least one second microelectronic device having an active surface and a back surface within said at least one opening such that said second microelectronic

device active surface resides adjacent said second microelectronic substrate core first surface;

disposing a second encapsulation material in said second microelectronic core opening adhering said second microelectronic substrate core to said at least one second microelectronic device, forming a first surface adjacent said second microelectronic active surface and a second surface adjacent said microelectronic die back surface; and

attaching said first microelectronic core to said second microelectronic core such that said first microelectronic device active surface oriented to face said second microelectronic device active surface.

37. The method of claim 36, further including forming an interconnection layer disposed proximate said first microelectronic substrate core first surface, said first encapsulation material first surface, and said first microelectronic device active surface and further including forming a second interconnection layer disposed proximate said second microelectronic substrate core first surface, said second encapsulation material first surface, and said first microelectronic device active surface; and wherein said attaching said first microelectronic core to said second microelectronic core includes forming electrical connections between said first and second interconnection layers.

38. The method of claim 36, further including forming an interconnection layer disposed proximate at least one of said first microelectronic substrate core second surface, said first encapsulation material second surface, and said first microelectronic

device back surface, and said second microelectronic substrate core second surface, said second encapsulation material second surface, and said second microelectronic device back surface.

39. The method of claim 36, further including forming at least one conductive via to extend from said first microelectronic substrate core first surface and said first microelectronic substrate core second surface.

40. The method of claim 36, further forming including at least one conductive via to extend from said second microelectronic substrate core first surface and said second microelectronic substrate core second surface.

41. The method of claim 36, further including forming at least one conductive via interconnecting said first microelectronic substrate core second surface and said second microelectronic substrate core second surface.

42. The method of claim 36, further including thermally attaching at least one heat dissipation device to at least one of said at least one first microelectronic device back surface and said at least one second microelectronic device back surface.

43. The method of claim 42, further including forming at least one conductive via interconnecting said first microelectronic substrate core first surface and said second microelectronic substrate core first surface.

44. The method of claim 43, further including disposing a dielectric material between said at least one conductive via and said heat dissipation device..